REMARKS

Claims 1-29 are pending. Claims 6 and 17 are canceled herein. Claims 1-5, 7-16 and 18-22 are amended herein. No new matter has been added as a result of these amendments.

CLAIM REJECTIONS - 35 U.S.C. § 112

The instant Office Action states that Claims 6-10 and 17-21 are rejected under 35 U.S.C. § 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter at issue. In particular, the instant Office Action points out that Claims 6 and 17 recite the feature "said instruction", for which there is insufficient antecedent basis.

Applicants respectfully point out that Claims 6 and 17 have been canceled herein. In so much as Claims 6 and 17 have been canceled, Applicants respectfully submit that the rejections of Claims 6 and 17 under 35 U.S.C. § 112 are moot at this time.

Moreover, Applicants respectfully point out that Claims 7-10 no longer depend from Claim 6, and that Claims 18-21 no longer depend from claim 17. In so much as Claims 7-10 no longer depend from Claim 6, and in so much as Claims 18-21 no longer depend from claim 17, Applicants respectfully submit that Claims 7-10 and 18-21 overcome the rejections under 35 U.S.C. § 112, and that these claims are in a condition for allowance as being dependent on an allowable

base claim. As such, allowance of Claims 7-10 and 18-21 is respectfully requested.

CLAIM REJECTIONS - 35 U.S.C. § 102(b)

The instant Office Action states that Claims 1-29 are rejected under 35 U.S.C. § 102(b) as being anticipated by Johnson et al. (*Cyclical Cascade Chains: A Dynamic Barrier Synchronization Mechanism for Multiprocessor Systems*; herein "Johnson"). Applicants respectfully point out that Claims 6 and 17 have been canceled herein. In so much as Claims 6 and 17 have been canceled, Applicants respectfully submit that the rejections of Claims 6 and 17 under 35 U.S.C. § 102(b) are moot at this time. Moreover, Applicants have reviewed Johnson and respectfully submit that the embodiments recited in Claims 1-5, 7-16 and 18-29 are not anticipated by Johnson for at least the following rationale.

Independent Claim 1, and similarly Claims 12 and 23, as amended, recites the features (emphasis added):

> A method of synchronizing a plurality of processors of a multi-processor computer system on a synchronization point, said method comprising:
>
> triggering a first set of processors to enter an entry holding loop in response to said first set of processors encountering said synchronization point before a lead processor associated with said plurality of processors;
>
> triggering said first set of processors to enter an exit holding loop in response to said lead processor encountering said synchronization point; and
>
> triggering said plurality of processors to leave said exit holding loop in response to a tail processor associated with said plurality of processors encountering said synchronization point.

MPEP § 2131 provides:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). ... "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim.

Applicants respectfully submit that Johnson fails to disclose each and every element of Claim 1, and similarly Claims 12 and 23. Applicants understand Johnson to teach "a processor may proceed if and only if it has reached the barrier and the processor numerically above it in its barrier group has also reached the barrier and may proceed." Johnson, page 4, column 1, paragraph 3 (emphasis added). Applicants further understand Johnson to teach "[t]o complete this initial static barrier and subsequent dynamic barriers, a processor executes a wait (next) routine, where next is a bit string indicating what processors it wants to have in its next group. Johnson, page 6, column 2, paragraph 3 (emphasis added).

Applicants do not understand Johnson to anticipate, for example, "triggering a first set of processors to enter an entry holding loop in response to said first set of processors encountering said synchronization point before a lead processor associated with said plurality of processors; triggering said first set of processors to enter an exit holding loop in response to said lead processor encountering said synchronization point; and triggering said plurality of

processors to leave said exit holding loop in response to a tail processor associated with said plurality of processors encountering said synchronization point", as claimed.

As stated above, Applicants understand Johnson to teach "a processor may proceed if and only if it has reached the barrier and the processor numerically above it in its barrier group has also reached the barrier and may proceed." Johnson, page 4, column 1, paragraph 3 (emphasis added). However, Applicants do not understand "a processor may proceed if and only if it has reached the barrier and the processor numerically above it in its barrier group has also reached the barrier and may proceed" to anticipate, for example, "triggering a first set of processors to enter an entry holding loop in response to said first set of processors encountering said synchronization point before a lead processor associated with said plurality of processors; triggering said first set of processors to enter an exit holding loop in response to said lead processor encountering said synchronization point; and triggering said plurality of processors to leave said exit holding loop in response to a tail processor associated with said plurality of processors encountering said synchronization point", as claimed (emphasis added).

Moreover, as stated above, Applicants understand Johnson to teach "[t]o complete this initial static barrier and subsequent dynamic barriers, a processor executes a wait (next) routine, where next is a bit string indicating what

processors it wants to have in its next group. Johnson, page 6, column 2, paragraph 3 (emphasis added). However, Applicants do not understand "[t]o complete this initial static barrier and subsequent dynamic barriers, a processor executes a wait (next) routine, where next is a bit string indicating what processors it wants to have in its next group" to anticipate, for example, "triggering a first set of processors to enter an entry holding loop in response to said first set of processors encountering said synchronization point before a lead processor associated with said plurality of processors; triggering said first set of processors to enter an exit holding loop in response to said lead processor encountering said synchronization point; and triggering said plurality of processors to leave said exit holding loop in response to a tail processor associated with said plurality of processors encountering said synchronization point", as claimed (emphasis added).

> The foregoing notwithstanding, the instant Office Action states:
>
> Regarding claims 6, 17 and 23, Johnson discloses the method of claim 5 further comprising enabling processors of said first set of processors to enter an entry holding loop if said processors of said first set of processors encounter said instruction before said lead processor [page 4, section 4, paragraph 1; sections 4 and 5; when a processor encounters a barrier point, the processor waits until all other processors associated with that barrier have reached the barrier point].

See the instant Office Action, page 5, section 13 (emphasis added). However, Applicants do not understand "when a processor encounters a barrier point, the processor waits until all other processors associated with that barrier have reached the barrier point" to anticipate, for example, "triggering a first set of

processors to enter an entry holding loop in response to said first set of processors encountering said synchronization point before a lead processor associated with said plurality of processors; triggering said first set of processors to enter an exit holding loop in response to said lead processor encountering said synchronization point; and triggering said plurality of processors to leave said exit holding loop in response to a tail processor associated with said plurality of processors encountering said synchronization point", as claimed (emphasis added). Instead, Applicants understand Johnson to be silent with respect to the combination of the above-recited claim features. Therefore, Applicants respectfully submit that the instant Office Action has not established a *prima facie* case of anticipation, pursuant to 35 U.S.C. § 102(b), at least because Johnson fails to teach each and every feature recited in Claim 1, and similarly Claims 12 and 23, as amended.

For at least the foregoing rationale, Applicants respectfully submit that Claim 1, and similarly Claims 12 and 23, as amended, is not anticipated by Johnson under 35 U.S.C. § 102(b). As such, allowance of Claims 1, 12 and 23 is respectfully requested.

With respect to Claims 2-5 and 7-11, Applicants respectfully point out that Claims 2-5 and 7-11 depend from allowable amended independent Claim 1, and recite further features. With respect to Claims 13-16 and 18-22, Applicants respectfully point out that Claims 13-16 and 18-22 depend from allowable

amended independent Claim 12, and recite further features. With respect to Claims 24-29, Applicants respectfully point out that Claims 24-29 depend from allowable independent Claim 23, and recite further features. Therefore, Applicants respectfully submit that Claims 2-5, 7-11, 13-16, 18-22 and 24-29 overcome the rejections under 35 U.S.C. § 102(b), and that these claims are thus in a condition for allowance as being dependent on an allowable base claim. As such, allowance of Claims 2-5, 7-11, 13-16, 18-22 and 24-29 is respectfully requested.

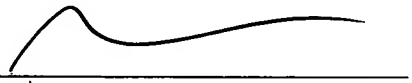
CONCLUSION

In light of the above-listed remarks, reconsideration of the rejected claims is requested. Based on the amendments and arguments presented above, it is respectfully submitted that Claims 1-29 overcome the rejections of record. Therefore, allowance of Claims 1-29 is respectfully solicited.

Should the Examiner have a question regarding the instant amendment and response, the Applicants invite the Examiner to contact the Applicants' undersigned representative at the below listed telephone number.

Respectfully submitted,
WAGNER BLECHER LLP

Date: 12/21/2007



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